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Docket No.: TESSERA 3.0-205 A DIV
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Beroz et al.

Application No.: Not Yet Assigned Group Art Unit: 3729

Filed: Herewith Examiner: M. Trinh

For: MICROELECTRONIC JOINING
PROCESSES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

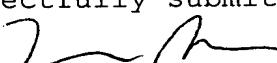
It is respectfully requested that the references listed on the enclosed form be made of record and considered with respect to the above-referenced U.S. patent application. A copy of each reference was of record in Application No. 09/523,513, the benefit of which is claimed under § 120. Submission of the present Information Disclosure Statement should not be taken as an admission that the cited references are legally available prior art or that the same are pertinent or material.

In the event that any fee is due in connection with the present Information Disclosure Statement, the Commissioner is hereby authorized to charge the same to our Deposit Account No. 12-1095.

Dated: August 26, 2003

Respectfully submitted,

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	Not Yet Assigned
				Filing Date	Concurrently Herewith
				First Named Inventor	Masud Beroz
				Art Unit	3729
				Examiner Name	M. Trinh
Sheet	1	of	2	Attorney Docket Number	TESSERA 3.0-205 A DIV

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	AA	US-5,133,495	07/1992	ANGULAS ET AL.	
	AB	US-5,148,265	09-15-1992	KHANDROS ET AL.	
	AC	US-5,148,266	09-15-1992	KHANDROS ET AL.	
	AD	US-5,203,076	04/1993	BANERJI ET AL.	
	AE	US-5,232532	08/1993	HORI	
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	AG	US-5,431,328	07/1995	CHANG ET AL.	
	AH	US-5,518,964	05-21-1996	DISTEFANO ET AL.	
	AI	US-5,578,527	11/1996	CHANG ET AL.	
	AJ	US-5,659,952	08-26-1997	KOVAC ET AL.	
	AK	US-5,706,174	01-06-1998	DISTEFANO ET AL.	
	AL	US-5,766,987	06-16-1998	MITCHELL ET AL.	
	AM	US-5,776,796-A1	07-07-1998	DISTEFANO ET AL.	
	AN	US-5,798,286	08-25-1998	FARACI ET AL.	
	AO	US-5,801,446	09-01-1998	DISTEFANO ET AL.	
	AP	US-5,834,339	11-10-1998	DISTEFANO ET AL.	
	AQ	US-5,843,251	12/1998	TSUKAGOSHI ET AL.	
	AR	US-5,861,678	01/1999	SCHROCK	
	AS	US-5,885,849	03/1999	DISTEFANO ET AL.	
	AT	US-5,915,752	02-03-1994	DISTEFANO ET AL.	
	AU	US-5,989,936-B1	11/1999	SMITH ET AL.	
	AV	US-6,189,208	02/2001	ESTES ET AL.	
	AW	US-6,324,754	12/2001	DISTEFANO ET AL.	
	AX	US-6,460,245	10/2002	DISTEFANO	

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)			
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449A/B/PTO				Complete if Known	
				Application Number	Not Yet Assigned
				Filing Date	Concurrently Herewith
				First Named Inventor	Masud Beroz
				Art Unit	3729
				Examiner Name	M. Trinh
Sheet	2	of	2	Attorney Docket Number	TESSERA 3.0-205 A DIV

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		
	CA	Multi-Chip Module Technologies and Alternatives: The Basics (Doame and Franzon, eds., 1993, pp. 450-476).		
	CB	RAMOS, RICHARD, Flux Free Process for Placement and Attach of Solder Balls to Wafers, Flip Chips and all BGA Packages.		
	CC	SOLBERG, Vern, Design Guidelines for Surface Mount and Fine Pitch Technology, 2d ed., Electronic Packaging and Interconnection Series.		

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